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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/238,262	01/27/99	SCHAEFER J	10191/955

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EXAMINER	
ALANKO, A	
ART UNIT	**PAPER NUMBER**
1746	7

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Please find below and/or attached an Office communication concerning this application or pr ceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No. 09/238,262	Applicant(s) SCHAEFER ET AL.	
	Examiner Anita K Alanko	Art Unit 1746	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/20/2000 amendment "a"* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Objections

1. Claim 5 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. It is not clear how an "integrated circuit photoresist technique" is different from or further limits a "photoresist technique." All photoresist techniques are integrated circuit photoresist techniques and vice versa.

Claim Rejections - 35 USC § 112

2. Claims 1-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 3, the term "edge areas" is indefinite. Are these edge areas the peripheral areas of the upper surface or bottom surface, a sidewall of a groove, or edges of the wafer, i.e., the side surface that connects the wafer bottom surface and the wafer top surface? For the purposes of the rejections below, the claim is considered to cite that that the edge area is the side surface that connects the wafer bottom surface and the wafer top surface.

In claim 1, lines 4-6, the phrase "the negative areas including the edge areas of the wafer" is unclear. Line 3 of the claim seems to define the edge areas as being separate from the surface

area, so it is unclear how the surface can include negative areas that are an edge because the surface is not an edge.

As to claim 5, the term "standard" is an indefinite term because standards change. It may be simply deleted.

Claims 2-4, 6-9 do not cure the indefiniteness of their base claim, and are therefore also rejected.

Claim Rejections - 35 USC § 103

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Renken et al (U.S. Patent No. 4542650).

Renken discloses a method (col.9, lines 24-32) comprising the steps of:

- providing a wafer having a surface and edge areas ("silicon substrate");
- dividing the surface of the wafer into positive areas (areas where the oxide layer has openings), to be subsequently etched in a wet chemical etching process, and negative areas including the edge areas of the wafer;
- providing the negative areas with a passivation layer ("photoresist is applied to all sides", exposed and developed) to protect the negative areas from the subsequent wet chemical etching process (Fig.3A);
- etching the wafer in a chemical etching process (col.9, lines 31-32); and
- removing the passivation layer ("resist is stripped").

Renken does not disclose that the etching process is a wet chemical etching process. Renken discloses that the etching process is an isotropic etching process. Examiner takes official

notice that isotropic etching processes are conventionally wet etching processes. It would have been obvious to one with ordinary skill in the art to use a wet chemical etching process in the method of Renken because isotropic etching processes are conventionally wet chemical etching processes.

4. Claims 1-3, 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Renken et al (U.S. Patent No. 4542650) in view of Pearce (U.S. Patent No. 5711891).

The discussion of Renken from above is repeated here. As to claims 2-3, Renken discloses to apply an oxide layer that is structured by using a photoresist and removed in subareas after the negative areas are provided and before the wafer is etched technique (col.9, lines 30-31). Renken does not disclose that the oxide layer can be a nitride layer.

Pearce teaches that the use of nitride layers over oxide layers is advantageous in order to have more dimensional stability during etching (Fig.3-4, col.1, lines 52-67). It would have been obvious to one with ordinary skill in the art to use a nitride layer instead of an oxide layer in the method of Renken because Pearce teaches that this provides for more dimensional stability during etching.

As to claim 5, the photoresist technique of Renken is an integrated circuit photoresist technique.

As to claims 6-7, Renken discloses to strip the photoresist after the structuring step, which encompasses removing after exposing and developing.

5. Claims 1-3, 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (U.S. Patent No. 5804090).

Iwasaki discloses a method (Fig. 15A-C) comprising the steps of:

- providing a wafer 30 having a surface and edge areas (Fig.15A);
- dividing the surface of the wafer into positive areas S2, to be subsequently etched in a wet chemical etching process, and negative areas (areas that are not to be etched) including the edge areas of the wafer;
- providing the negative areas with a passivation layer 33, 34 to protect the negative areas from the subsequent wet chemical etching process (Fig.15A, col.26, lines 12-15);
- etching the wafer in the wet chemical etching process (Fig.15B, col.26, lines 16-22); and

Iwasaki does not disclose to remove the passivation layer. It would have been obvious to one with ordinary skill in the art to remove the passivation layer in the method of Iwasaki because it is conventional to remove layers that are not required as a part of the final device, such as etch masks.

As to claims 2-3, Iwasaki discloses in another embodiment to form a further mask 37 in at least subareas of the positive areas (Fig. 20, col.28, lines 24-26). Iwasaki does not disclose that the mask is a nitride layer since Iwasaki does not disclose the composition of the mask 37. Iwasaki discloses that the use of silicon nitride layers as masking layers is known (col.20, line 20). Iwasaki also discloses to use silicon nitride rather than silicon oxide layers because they can be formed to smaller thicknesses which improves processing etch times in aqueous KOH (col. 3, lines 53-65); It would have been obvious to one with ordinary skill in the art to use a nitride layer as the mask 37 in the method of Iwasaki to define part of the positive areas because Iwasaki teaches that they are conventional etch mask layers.

Iwasaki does not disclose how to structure the mask to form the pattern (Fig.19A,B). Examiner takes official notice that it is conventional in the art to pattern nitride layers by using a photoresist technique, such as an integrated circuit photoresist technique that uses exposing and developing steps. It would have been obvious to one with ordinary skill in the art to use a photoresist technique with exposing and developing to pattern nitride layer as a mask 37 in the method of Iwasaki because it is conventional in the art.

As to claims 5-7, see the rejection of claims 2-3. Examiner takes official notice that it is conventional in the art to remove photoresist after patterning an underlying layer, such as a nitride layer. It would have been obvious to remove the photoresist after exposing and developing in the method of Iwasaki because it is conventional to remove a photoresist layer after patterning an underlying layer.

As to claim 8, Iwasaki discloses that the passivation layer 33, 34 is an oxide layer (col.26, lines 9-15).

As to claim 9, Iwasaki s discloses that the oxide layer is formed on the wafer (col.5, lines 24-25), but does not disclose that a LOCOS process is used. Examiner takes official notice that it is conventional in the art to form oxide layers by a LOCOS process. It would have been obvious to one with ordinary skill in the art to use a LOCOS process to form the oxide layer in the method of Iwasaki because it is a conventional technique for forming oxide layers.

6. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (U.S. Patent No. 5804090) in view of O'Neill (U.S. Patent No. 5131978).

The discussion of Iwasaki from above is repeated here.

As to claim 4, Iwasaki does not disclose to apply a further passivation layer in subareas. O'Neill discloses a method for the fabrication of three dimensional structures from silicon comprising the steps of:

- providing a wafer 10 having a surface (Fig.3A);
- dividing the surface of the wafer into positive areas 20 (unmasked areas), to be subsequently etched in a wet chemical etching process, and negative areas (masked areas);
- providing the negative areas with a passivation layer 30, 32 to protect the negative areas from the subsequent wet chemical etching process (Fig.3A);
- etching the wafer in the wet chemical etching process (Fig.3D, col.5, line 53); and
- removing the passivation layer (Fig.3F, col.6, lines 25-27).

O'Neill discloses to divide the wafer into positive and negative areas by:

- applying a nitride layer 30 (col.5, line 5); and
- structuring the nitride layer 18 using a photoresist technique (col.5, line 11) so that the positive areas are defined by a part of the surface covered with the nitride layer;
- removing the nitride layer at least in subareas of the positive areas (where channel 20 is to be etched), after the negative areas are provided and before the wafer is etched (Fig.3B);
- applying a further passivation layer 38 (col.5, lines 26-28) in the subareas, after the removal of the nitride layer 30 in the subareas and before the wafer is etched; and
- completely removing the nitride layer (Fig.3F).

It would have been obvious to one with ordinary skill in the art to apply a further passivation layer and to remove the nitride layer in the method of Iwasaki as taught by O'Neill

because O'Neill teaches that this is a conventional technique for patterning three dimensional structures in silicon by etching.

Response to Amendment

7. The 35 U.S.C. 112, second paragraph rejection of claim 4, the rejection of claims 1-8 under 35 U.S.C. 102(b) as being anticipated by O-Neill (U.S. Patent No. 5131978), the rejection of claims 1-3, 5-8 under 35 U.S.C. 102(e) as being anticipated by Burns et al (U.S. Patent No. 5738757), and the rejection of claims 1-3, 5-9 under 35 U.S.C. 103(a) over Burns et al (U.S. Patent No. 5738757) are withdrawn.

8. Claim 5 is objected to and claims 1-9 are rejected under 35 U.S.C. 112, second paragraph. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Renken et al (U.S. Patent No. 4542650). Claims 1-3, 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Renken et al (U.S. Patent No. 4542650) in view of Pearce (U.S. Patent No. 5711891). Claims 1-3, 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (U.S. Patent No. 5804090). Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (U.S. Patent No. 5804090) in view of O'Neill (U.S. Patent No. 5131978).

Response to Arguments

9. The rejections over Burns and O'Neill are withdrawn. Examiner misunderstood the claims: Burns and O'Neill do not teach the step of providing the edge areas of the wafer with a passivation layer. The figures of Burns and O'Neill do not show the edge of the wafer, therefore

it is unclear whether the edge areas are covered with a passivation layer or not. Therefore, the claims are now rejected over Iwasaki and Renken, whom both clearly teach to passivate all sides of the wafer, including edge areas.

Applicant's arguments are not persuasive as they apply to Iwasaki modified by O'Neill. Applicant argues that O'Neill teaches away from having positive areas and negative areas defined prior to any etching. However, the areas are necessarily defined prior to etching because the etch mask is not randomly exposed, it is exposed and developed using a predefined mask to obtain a predefined pattern. They are therefore defined prior to etching.

As to the objection of claim 5, applicant submits that the term "standard" further limits the base claim. However, this is not persuasive because applicant has not shown how an "integrated circuit photoresist technique" is different from, and further limits a "photoresist technique."

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita K Alanko whose telephone number is 703-305-7708. The examiner can normally be reached on Monday-Friday, 9:30-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Randy Gulakowski can be reached on 703-308-4333. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-7719 for regular communications and 703-305-3599 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Anita Alanko
Patent Examiner
Art Unit 1746

AKA
January 24, 2001